* * * R*E*M*A*R*K*S * * *

Applicants herewith submit this RESPONSE B, a Response After Final Action, in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicants respectfully request this Response B be entered and further request re-examination and reconsideration of the above referenced patent application in view of the remarks as set forth below. If allowance of the claims is not forthcoming as a consequence of this Response B, then it will, in any case, put the application in a better condition for consideration on appeal.

Rejections under 35 U.S.C. §§102

The Examiner has again rejected claims 1 through 16 under 35 U.S.C. § §102(b) as being anticipated by United States Patent No. 6,072,340 issued on June 6, 2000 to Cecil W. Deisch (Deisch). The Examiner has recited a number of rejections for Applicant's Claims 1 through 16. Applicant will consider each rejection of each claim independently.

Applicant has very carefully studied the disclosure by Deisch. In general and applicable to Applicant's Claims 1 through 16 there is a basic and fundamental difference between the claimed invention and the apparatus disclosed by Deisch. Applicant claims apparatus and method for measuring characteristics of a bit stream of binary pulses. In contrast, Deisch teaches a pulse shaping and filtering circuit for digital pulse data transmissions. This goes to the heart of the matter. In the Deisch statement

of background of the invention Deisch indicates that the essential purpose of his invention is the need to shape and filter digital pulse transmissions. Thus, Deisch as set forth in his brief summary of the invention, discloses a signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream. The claims of Applicant's invention recite apparatus and method for measuring characteristics of a bit stream of binary pulses; a totally different concept from that taught by Deisch.

The Examiner's attention is directed toward a basic electrical engineering text by Gladwyn V. Lago and Donald L. Waidelich entitled "Transients in Electrical Circuits" published by The Ronald Press Company, New York, 1958, especially chapters 14 through 16 explaining basic Fourier integrals that are the basis for the pulse shaping apparatus disclosed by Deisch and the output waveforms therefrom.

Applicants respectfully traverse rejection of Claim 1. In rejecting Claim 1, the Examiner states that Deisch discloses an apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator. Contrary to the Examiner's statement, Deisch's abstract very clearly states "A pulse shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream is set forth ....". A very careful reading will show that nowhere does the Deisch abstract, disclosure or drawing, disclose teach, suggest or in any way anticipate Applicant's novel apparatus recited in Claim 1 for measuring characteristics of a bit stream of binary pulse transmissions. The Examiner further states that Deisch discloses Applicant's

recited control means for defining a window comparator. Nowhere does Deisch in his abstract, disclosure or drawing disclose teach, suggest or in any way anticipate Applicant's novel control means recited in Claim 1 for defining a window comparator. Deisch's Fig. 7 is only a graph of the output of his pulse shaping circuit Fig. 6, not a window comparator. Applicant submits that nowhere in the Deisch disclosure, drawing or abstract does he disclose teach, suggest or in any way anticipate the control means recited in Claim 1 for defining a window comparator.

Applicant's Claim 1 further recites "... logic means for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics....". The Examiner states that Deisch discloses Applicant's recited logic means. It is respectfully submitted that Deisch does not disclose a window comparator and thus cannot accumulate event counts of the bit stream pulses falling within points inside the window comparator. A very careful reading of the Deisch disclosure reveals that the pulse shaping apparatus taught by Deisch is not similar to or performs the functions of Applicant's recited novel logic means. Applicant submits that nowhere in the Deisch disclosure does Deisch disclose teach, suggest or in any way anticipate the logic means recited in Claim 1. Deisch discloses a pulse shaping apparatus, the crux of his invention, not the logic means recited in Claim 1.

In view of the above, it is submitted that independent Claim 1 and dependent Claims 2 through 6, further defining the novel structure recited in Claim 1, are neither taught nor anticipated by the Deisch reference and Claims 1 through 6 are therefore clearly allowable under 35 U.S.C. §102(b). It is respectfully submitted that the Deisch reference is too remote and does not give rise to a §102, nor for that matter a §103, rejection of Applicant's novel Claims 1 through 6.

Applicants respectfully traverse rejection of Claim 7. In rejecting Claim 7, the Examiner again states that Deisch discloses an apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator. Contrary to the Examiner's assertion, in Deisch's brief summary of the invention, Deisch states, as does in his abstract, that his invention is for a signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream....", col. 2, ll. 41 and 42. Note Deisch's statements, col. 4, ll. 51 and 52, saying that Fig, 8 illustrates a pulse shaping circuit, and col. 5, ll. 48 and 49 saying that Fig. 10 is a filtering and shaping circuit. Thus, Deisch's Figs, 6, 8 and 10 are, in his words, pulse shaping circuits, not Applicant's recited control means of Claim 7 for defining a window comparator used in Applicant's claimed apparatus for measuring characteristics of a bit stream of binary pulses. See fig. 3-3-1, page 66, and others of the aforementioned text by Lago and Waidelich for a basic understanding of the operation of these types of Deisch's circuits.

The Examiner also states Deisch discloses a window comparator of an array of columns and rows defining points for accumulating voltage counts of a binary pulse bit stream. Deisch does not disclose, teach or anticipate Applicant's claimed control means recited in Claim 7 for defining a window comparator of an array of columns and rows defining points for accumulating voltage counts of the binary pulse bit stream. Again Deisch in his own words only teaches pulse shaping circuits. Applicant's Claim 7 recites novel apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses. It must be noted that Deisch is silent in this regard.

Deisch Fig. 7 shows a plotted output of his Fig. 6 ideal pulse shaping circuit wherein the output 122 is the straight S_{OUT} line of the graph set forth in Fig. 7. Col. 2 and 3, ll. 40 through 7, set forth the operation of his apparent pulse shaping apparatus. It is submitted that this information of Deisch's disclosure does not disclose, teach or anticipate in any way Applicant's claimed apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels. Again Deisch's

Figs. 8 and 10 are in his own words pulse shaping circuits. Deisch's Figs. 7, 9G and 11B are the outputs of pulse shaping circuits 6, 8 and 10 respectively. Fig. 11A is apparently an input to his pulse shaping circuit 10. Again, Deisch's pulse shaping apparatus does not disclose, teach or anticipate in any way Applicant's Claim 7 recitation of control means for defining a window comparator and apparatus that creates a voltage threshold window that moves between minimum and a maximum voltage levels and accumulates counts of voltage levels of the binary pulses and displays the accumulated time and voltage counts as an eye diagram defining characteristics of a bit stream of binary pulses. Deisch only discloses pulse shaping circuits in Figs. 8 and 10 and outputs therefrom in graphs of Figs. 9G and 11B. Deisch does not disclose apparatus for displaying an eye diagram defining characteristics of a bit stream of binary pulses. Deisch only discloses graphs showing the output of pulse shaping circuits set forth in his Figs. 6, 8 and 10. It is to be noted that graph set forth in Fig. 5 is not an eye diagram but only illustrates the straight line S_{OUT} resulting from the charging of the capacitor C set forth in the circuit of Fig. 4.

In view of the above set forth arguments it is submitted that independent Claim 7 is neither taught nor anticipated by the Deisch reference and Claim 7 is therefore clearly allowable under 35 U.S.C. §102(b). It is respectfully submitted that the Deisch reference is too remote and does not give rise to a §102,nor for that matter a §103 rejection of Applicant's novel Claim 7.

Applicants respectfully traverse rejection of Claim 8. In rejecting Claim 7, the Examiner again states that Deisch discloses an apparatus for measuring characteristics of a bit stream of binary pulses including first control means for defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream. As set forth above, Deisch discloses pulse shaping circuits and does not disclose, teach or anticipate Applicant's first control means recited in Claim 8 for defining a window comparator of an array. The Examiner's attention is directed to the first line of the Deisch abstract wherein Deisch clearly states "A signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream is set forth....".

Applicant's Claim 8 further recites "... second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array....". Deisch's Fig. 7 sets forth a graph illustrating a straight line output S_{OUT} of his idealized pulse shaping circuit set forth in Fig. 6, wherein the output V_{OUT} of the pulse shaping circuit of Fig. 6 is the straight line output S_{OUT}. This is a teaching in an opposite direction from the second control means to the extent it is relevant at all.

Figs. 6 & 7 of Deisch and the disclosure relating thereto do not support the Examiner's assertion that Applicant's claimed first or second control means for creating a voltage threshold window that moves between a minimum and maximum voltage

threshold with each row of the array as set forth in Claim 8 is in any way disclosed, taught or anticipated by this or any other section of Deisch. Applicant has reviewed and studied Deisch carefully and does not find where Deisch teaches a voltage threshold window that moves between a minimum and maximum voltage threshold. The Examiner's assistance in drawing the Applicant's attention to the precise location where this is found is requested. Column and line number would be appreciated. Moreover, Applicant requests that the Examiner point out precisely where in the Deisch disclosure and drawings, there is disclosed the minimum and maximum voltage thresholds. Applicant again has reviewed and studied Deisch carefully and it does not appear to Applicant to be in the Deisch disclosure.

Applicant's Claim 8 recites "...logic means for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold at each row and column point of the array....". Deisch's disclosed pulse shaping and filtering apparatus 100 has a one bit shift register 106 set forth in his Fig. 8 pulse shaping circuit for detecting a binary pulse all the time. This is completely unlike Deisch, where register 106 pays no attention to when the pulse voltage levels are within the voltage threshold at each row and column point of an array.

Again, Applicant's claimed logic means does pay such attention and this limitation is found nowhere in Deisch. In fact, Deisch seems to be a teaching in an opposite or at least divergent direction. In fact, based upon the Deisch disclosure there

is no teaching of how the register detects binary pulse voltage levels within the voltage threshold. Again, there is no first control means for defining a window comparator and second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array. It is respectfully submitted that Deisch does not disclose, teach or anticipate Applicant's first and second control or logic means as recited in Claim 8. Applicant respectfully submits that Deisch does not disclose any counter means, let alone Applicant's claimed first and second counter means.

Deisch's Fig 7 is a plotted graph showing the waveforms of his pulse shaping circuit set forth in Fig. 6. Contrary to the Examiner's statement, Deisch does not disclose any counting means. Again, Applicant has carefully reviewed the Deisch disclosure and finds no mention of such counting means. The Examiner's assistance in reciting Column and line numbers is requested.

The pulse shaping circuits of Deisch's Figs. 6 and 8 appear to continuously generate a straight line and harmonic outputs, respectively, and there is no apparatus for accumulating counts of outputs of anything. Fig. 7 is merely a plot of the straight line output S_{OUT} of pulse shaping circuit of Fig. 6. Applicant submits that Deisch does not disclose any such counting means let alone Applicant's first and second counter means. In contrast to Applicant's recited second counter means for accumulating the detected binary pulse voltage levels at each point of the array, Deisch's graph set forth

in his Fig. 5 is merely a graph, not of the pulse levels, but of constant voltage output V_{OUT} of the charge of capacitor C of the circuit of Fig. 4. Deisch does not disclose Applicant's claimed monitor apparatus of Claim 8. It is respectfully submitted that Deisch doesn't disclose any monitor apparatus. It is also submitted that Deisch does not disclose, teach or anticipate in any an apparatus for displaying an eye diagram defining characteristics of a bit stream of binary pulses. It is submitted that the graphs of Figs. 5 and 7 are not eye diagrams but merely plotted graphs of the straight line voltage output of the voltage of capacitors C of the pulse shaping circuits of Figs. 4 and 6.

It is further submitted that the reference of Deisch does not disclose, teach or anticipate in any way the preamble of Applicant's Claim 8 and also does not disclose any of the claimed first and second control means, logic means, first and second counter means or monitor apparatus. In fact, Deisch appears completely silent with regard to these elements of Applicant's claims.

In view of the above set forth arguments it is submitted that independent Claim 8 is neither taught, disclosed nor anticipated in any way by the Deisch reference and Claim 8 is therefore clearly allowable under 35 U.S.C. §102(b). It is respectfully submitted that the Deisch reference is far too remote to the art of Applicant's Claim 8 for even §103.

Applicants respectfully traverse rejection of independent Claim 9 and dependent Claims 10 through 14. Applicant's Claim 9 recites "A method for determining characteristics of a bit stream of binary pulses comprising the steps of defining a window comparator and accumulating event counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream at points inside the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics." In rejecting Claim 9, the Examiner states that Deisch discloses a method for determining characteristics of a bit stream of binary pulses. Applicant respectfully submits that contrary to the Examiner's statement, Deisch in his own words, col. 2, ll. 41 and 42 of his brief summary of the invention, discloses a signal shaping circuit for shaping amplitude shift keyed digital pulses of a digital data stream. Even a cursory review of the above referenced basic text by Lago and Waidelich reveals the harmonics that comprise a digital pulse. Deisch apparently discloses circuits that generate harmonics that comprise the input digital pulses and filters out ones of the generated higher frequency harmonic signals to generate an output signal having a lower bandwidth than the input signal, col. 3, ll. 65 and 66 of his brief summary of the invention. Deisch's apparatus may respond to various distortions of the input digital signal by generating the same shaped output signal of the basic harmonics included in the overall harmonics comprising the input pulse signal. Since these higher frequency harmonic signal define characteristics of a binary pulse signal and are filtered out by the

Deisch apparatus, Deisch does not and by it own statements can not disclose Applicant's method for determining characteristics of a bit stream of binary pulses.

Applicant's Claim 9 recites a novel method for determining characteristics of a bit stream of binary pulses. Furthermore, Applicant's Claim 9 recites a step of defining a window comparator. As set forth above, Deisch, again, is completely silent in this regard. Deisch, col. 4, ll. 49 through 67, disclose a pulse shaping circuit, Fig. 8, apparently generating an output basic harmonic waveform plotted in his graph of Fig. 9G. A careful reading of Deisch's recitation set forth in col. 4, ll. 49 through 67, fails to disclose Applicant's step recited in Claim 9 for defining a window comparator. In addition, Deisch does not disclose, teach or anticipate in any way Applicant's method as recited in Claim 9 for accumulating event counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream at points inside the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics.

Deisch's brief summary of the invention, col. 2 and 3, ll. 40 through 7, discloses a broad concept of his pulse shaping circuits set forth in his Figs. 4, 6 and 8 and which outputs thereof are plotted in his graphs of Figs. 5, 7 and 9. As earlier set, Fig. 5 is not an eye diagram but simply plots the combined charge of capacitor C of the circuit set forth in Fig. 4 as a straight line voltage output S_{OUT}. Similarly, Fig. 7 is not an eye diagram but simply plots the combined charge of capacitor C of the circuit set forth in

Fig. 6 as a straight line voltage output S_{OUT}. Note that if Deisch had disclosed a monitor connected to the output of the idealized circuits set forth in Figs 4 and 6 the view would simply be the straight ll. S_{OUT}. Note also that the graph of Fig. 9G does not illustrate an eye diagram but simply the basic harmonics of the digital pulse signal applied to his pulse shaping circuit of Fig. 8. Thus, Deisch does not disclose, teach or anticipate Applicant's preamble or steps of defining a window comparator or accumulating event counts of the bit stream pulses and drawing an eye diagram therefrom defining the bit stream pulse characteristics. Deisch is totally silent in all regards with respect to the preamble and elements recited in Applicant's Claim 9.

In view of the above set forth arguments it is submitted that independent Claim 9 and dependent Claims 10 through 14, further defining the steps of the method recited in Claim 9, are neither taught nor anticipated by the Deisch reference and Claims 9 through 14 are therefore clearly allowable under 35 U.S.C. §102(b). It is respectfully submitted that the Deisch reference is too remote and does not give rise to a §102, nor for that matter, a §103 rejection of Applicant's novel Claims 9 through 14.

Applicants respectfully traverse rejection of independent Claim 15. As repeatedly set forth above, Deisch discloses an apparatus for shaping input digital pulses. Deisch does not disclose a method for determining characteristics of a bit stream of binary pulses. It appears to Applicant that Deisch's pulse shaping circuit outputs are basic harmonics of the digital pulse input signals and do not determine

characteristics of a bit stream of binary pulses. Thus, Deisch does not disclose the preamble of Applicant's novel Claim 15 and is clearly in a field of art far different than Applicant's. Deisch also does not disclose Applicant's step of defining a window comparator of an array of columns and rows defining points for accumulating event counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream. Deisch's Fig. 7 is a plot of a graph of the output of his circuit set forth in his Fig. 6. There is no apparatus in his disclosure for defining a window comparator. Nor are there any comparator points in his plotted graph of Fig. 7 for accumulating event counts of multiple pulses of a binary pulse bit stream. Deisch is purposely silent (especially in his brief summary of his invention, col. 2, l. 40 through col. 3, line 6) in regard to the window defining step of Claim 15. There is no disclosure in Deisch regarding Applicant's recitation of defining points for accumulating event counts of the binary pulse bit stream. Nor does Deisch disclose Applicant's novel step for creating a voltage threshold window that moves between a minimum voltage and a maximum at each row of the array. Deisch's Fig. 9G is a plot of the basic harmonic signal generated by the pulse shaping circuit of Fig. 8. Fig. 10 is only another embodiment of Deisch's pulse shaping circuit. Applicant submits that there is no disclosure of a created voltage threshold window that moves between a minimum voltage and a maximum at each row of an array as set forth in Applicant's Claim 15.

Applicant's Claim 15 recites a step of accumulating counts of voltage levels of the binary pulses occurring at time when the pulse voltage levels are within the voltage threshold window at each point of the array and displaying the array accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses. As repeatedly set forth, Deisch's graph set in Fig. 7 is a plot of the wave forms generated by his circuit of Fig. 6. The points Deisch's waveforms do not appear to be accumulated counts of voltage levels of the binary pulses generated by operation of the S1 and S2 switches set forth in his Fig. 6 circuit. It is again submitted that Deisch does not disclose, as recited by Applicant's Claim 15, accumulated events counts of voltage levels of the binary pulses. If the Examiner believes to the contrary, Applicant requests the precise col. and line number for the disclosure.

It is submitted that the points in Deisch's graph of Fig. 7 are not counts of voltage levels of the binary pulses generated by operation of his S1 and S2 switches of the circuit of Fig. 6 but rather the charge of capacitor C. If the output plotted in Fig. 7 were set forth on a monitor, which Deisch does not disclose, it would not be an eye diagram but simply the straight line S_{OUT}. It is submitted that Deisch does not disclose, teach or anticipate any way Applicant's accumulating counts step (Claim 15), the steps of defining a window comparator, creating a voltage threshold window or accumulating event counts of the bit stream pulses and drawing an eye diagram therefrom defining

the bit stream pulse characteristics (also, Claim 15) (See Deisch col. 4, ll. 49 through 67 or Fig. 7).

In view of the above set forth arguments it is submitted that independent Claim 15 is not disclosed, taught nor in any way anticipated by Deisch. Therefore, Claim 15 is clearly allowable under 35 U.S.C. §102(b). It is respectfully submitted that Deisch is in an art class so far remote from Applicant's invention that it can not even give rise to a rejection under §103 when compared with Applicant's Claim 15.

Applicants respectfully traverse rejection of independent Claim 16. As set forth above, Deisch discloses an apparatus for shaping input digital pulses. Deisch does not disclose a method for determining characteristics of a bit stream of binary pulses. It appears that the Deisch pulse shaping circuit outputs an amplitude shift keyed data stream of basic harmonic signals having a lower bandwidth than the input signal. In Deisch application, as seen in Fig. 12, an output filter 305 generates a pulse shaped signal of a basic harmonic signal and filters in the receive circuit. These appear to completely eliminate the characteristics of the pulse signal on the transmission medium that are determined by Applicant's method (Claim 16). This is of course true as well for Claims 1 through 15.

Again, Deisch's graph of Fig. 7 is simply a plot of the voltage appearing on capacitor C and does not anticipate Applicant's recited window comparator of an array defining points for accumulating event counts. Deisch is purposely silent in this regard

(col. 2, ll. 40 through 67). If Deisch had disclosed monitoring apparatus the monitor would simply show the straight line output S_{OUT}. Again Deisch does not disclose the Claim 16 step of defining a window comparator of an array defining points for accumulating event counts during defined duration times of the binary pulse bit stream. Fig. 7 and the brief summary of the invention of Deisch are purposefully silent (col. 2, ll. 40 through 67). If Deisch were to disclose these elements of Applicant's claims, one would expect to find at least in these locations.

It is submitted that Deisch does not disclose Applicant's claimed steps of creating a voltage threshold window that moves between defined voltage levels at each row of the array or detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array. Again, Deisch's Fig. 7 is merely a plot of predicted voltage charges of capacitor C of his circuit of Fig. 6. There is no created threshold window, recited by Applicant, moving between defined voltage levels nor does he disclose Applicant's step of detecting voltage levels of binary pulses within the voltage threshold window at each row and column point of the array. He is totally silent in this regard. The Deisch plotted graph of his Fig.7 does not accumulate counts of the detected binary pulse voltage levels. At most, the plotted graph illustrates single, not accumulated, voltage points predicted as appearing on capacitor C of the circuit in Fig.6.

Deisch does not disclose Applicant's Claim 16 step of displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses. Figs. 7 – 10 would normally be expected to disclose such elements had Deisch meant his invention to have them. The fact that these elements are absent is clear and convincing evidence that Deisch does not disclose them.

Deisch does not disclose, teach or anticipate in any way the subject matter of Applicant's Claim 16. For example, Applicant's preamble states, "A method for determining characteristics of a bit stream of binary pulses, . . ." As noted above, Deisch doesn't even remotely relate to such an art.

Additionally, the steps of defining a window comparator, creating a voltage threshold window, detecting voltage levels of the binary pulses occurring within the voltage threshold window at, accumulating counts of the detected binary pulse voltage levels in a column and row point of the array, and displaying the array column and row points of the accumulated counts as an eye diagram defining characteristics of the bit stream of binary pulses. Deisch is devoid of any disclosure of any kind relating to this subject area.

In view of the above set forth arguments it is submitted that independent Claim 16 is not disclosed, taught or anticipated in any way by Deisch compared to Claim 16 and therefore Claim 16 is clearly allowable under 35 U.S.C. §102(b). It is also

respectfully submitted that Deisch is far too remote to give rise to a §103 based not only by the lack of elemental disclosure, but even a cursory reading of the Applicant's preamble for Claim 16.

Applicants respectfully traverse rejection of dependent Claims 2 through 6 and dependent Claims 10 through 14. Claims 2 through 6 define further the structure of parent Claim 1 and are clearly allowable under both §§102(b) and 103 in view of Deisch. For similar reasons, dependent Claims 10 through 14, which further define the method of parent Claim 9, are also clearly allowable as is Claim 9 under both §§102(b) and 103 in view of Deisch.

With regard to dependent Claims 2 through 6. Deisch, col. 4, line 57, discloses in Fig. 8, a delay circuit 106, which are arguably in his words, col. 5, line 2, a one bit shift register. Applicant's claimed programmable means; as recited in Claim 2 establishes an array defining points for accumulating counts of pulse voltage levels and for creating a voltage threshold window that moves between a minimum and maximum voltage. This is clearly not a one bit shift register. It is respectfully submitted that such register is incapable of performing the functions recited. If the Examiner disagrees, Applicant requests how such a one bit shift register could possibly function to establish an array defining points for accumulating counts of pulse voltage levels and for creating a voltage threshold window that moves between a minimum and maximum voltage. Clearly, this claim is allowable over Deisch.

Deisch does not disclose logic circuitry of the kind recited in Applicant's Claim 3 for detecting voltage levels of the binary pulses occurring at various time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array as set forth in parent Claim 2. The circuits in Figs. 6, 8 and the graph in Fig. 7 of Deisch, do not show this feature of Applicant's invention as recited in Claim 3. Claim 3 is thus clearly allowable over the Deisch whether with reference §102(b) or §103.

Deisch does not disclose the first and second counter means recited in Applicant's dependent Claims 4 and 5. These counter means accumulate counts of the detected binary pulse voltage levels in a column and row point of the array and define duration times of the bit stream of binary pulses to accumulate the counts of the detected binary pulse voltage levels falling within the voltage threshold window at each point of the array. Again, Applicant requests the Examiner to point specifically where in Deisch such counters or counter means are found. Claims 4 and 5 are clearly allowable over Deisch whether with reference to §102(b) or §103.

Deisch does not disclose the apparatus recited in Claim 6 for displaying array column and row points of accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses. Deisch does not disclose any display apparatus for displaying an eye diagram of any kind. Figs. 7 and 9 of Deisch are not eye diagrams. These figures are merely graphs plotted independently of

display apparatus. A careful examination of Deisch fails to show any recitation of any display apparatus let alone Applicant's claimed display apparatus. Claim 6 further defines the structure of parent Claims 1 through 5 is allowable in addition to Claims 1 through 5 over the Deisch reference whether with reference to §102(b) or §103.

With regard to dependent Claims 10 through 14. Deisch does not disclose, teach or even suggest the recitation in Claim 10 of a step of establishing an array of columns and rows defining the points for accumulating the event counts at time offsets during the defined duration times. As noted above, Fig. 7 is a graph plotting wave forms apparently generated the Fig. 6 circuit of Deisch. Deisch plots points of what appears to Applicant to be a single event. A single event is NOT an accumulated event and does not disclose, teach, anticipate or even suggest accumulated events. Claim 10 is clearly allowable whether with reference to §102(b) or §103.

Deisch does not does not disclose, teach, anticipate or even suggest the step recited in Applicant's Claim 11. Namely, wherein the window comparator defining step comprises the step of creating a voltage threshold window that moves with respect to a minimum and maximum voltage threshold wherein the voltage threshold window changes with respect to the rows of the array. Fig. 7 of Deisch is a graph plotting wave forms apparently generated by the circuit of Fig. 6. According to Deisch at col. 4, ll. 43 and 44, it maintains a generally constant output equal to the first peak 53 of the first signal S_{TO}. Claim 11 is clearly allowable whether with reference to §102(b) or §103.

Applicant also submits that Deisch does not disclose the step recited in Applicant's Claim 12 of detecting voltage levels of the binary pulses occurring at the time offsets of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array. Fig. 7 is a graph plotting wave forms apparently generated the circuit of Fig. 6. The Fig. 6 circuit generates a constant output S_{TO} in response to the operation of his switches S1 and S2. Since Deisch does not disclose a moving threshold window, there is no disclosure or teaching or even a suggestion of any kind of detecting voltage levels of the binary pulses of a bit stream when the pulse voltage levels are within the voltage threshold window. Claim 12 is clearly allowable whether with reference to §102(b) or §103.

Deisch does not disclose the steps recited in Applicant's Claims 13 and 14 for accumulating counts of the detected binary pulse voltage levels of a binary pulse bit stream and displaying column and row points of accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses. Again, Fig. 7 is a graphical plot of voltage forms generated by the simple circuit of Fig. 6. The Fig. 6 circuit does not measure pulses of a bit stream but responds to the battery voltages V1 and V2 in response to the operation of switches S1 and S2. The plotted graph of Fig. 7 does not accumulate detected binary pulse voltage levels in a column and row point of the array nor does it display the array column and row points of accumulated counts as an eye diagram defining characteristics of a bit stream of binary pulses. As set forth

above, there is no disclosure of any apparatus for displaying the straight line voltage S_{OUT} of the voltage appearing on the capacitor C of Fig. 6. Claims 13 and 14 are clearly allowable whether with reference to §102(b) or §103.

Although the Examiner does not identify specific claims in section 2 of his final office action, paragraphs A through H, Applicant traverses these arguments and responds to the Examiner's comments as follows:

Applicant's novel claimed invention discloses and teaches apparatus and method for measuring and determining characteristics of a bit stream of binary pulses. Oftentimes when a bit stream of binary pulses are applied to a transmission facility errors occur in the bit stream of binary pulses that are caused by the character of the transmission facility. Accordingly, apparatus and method is recited by Applicant's claims for measuring and determining characteristics of a bit stream of binary pulses transmitted on a transmission facility and which may be deformed by errors caused by the transmission facility. Specifically, Applicant claims a patentable apparatus and method for measuring and determining characteristics of a bit stream of binary pulses transmitted along a transmission facility. In the measuring operation, Applicant's claimed control structure defines a window comparator and logic structure for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and draws eye

diagrams therefrom defining the bit stream characteristics. Thus, the eye diagram shown is a measure of the continuous characteristics of the binary pulse bit stream.

Deisch is apparently concerned with errors occurring with binary bit pulses transmitted at high speeds on transmission facilities. Deisch realizes, as is basic electrical engineering knowledge (Gladwyn Lago and Donald L. Waidelich, supra) that a binary pulse may be symbolized by harmonic transients represented by multiple sinusoidally shaped waves that appear in increased frequencies depending on the period and configuration of the binary pulse. Thus, it appears that Deisch has determined that a high speed pulse can be shaped into transient pulses that are then filtered (Fig. 12) so that the lowest frequency pulse can by applied to a transmission facility 315. Thus, a high speed binary pulse is shaped and filtered into the lowest frequency harmonic waveform (Fig. 9C) that can be transmitted over a lower speed transmission facility.

There is a basic and fundamental distinction between the Applicant's claimed invention and Deisch. Applicant's claims are directed to a method for determining and apparatus for measuring characteristics of a bit stream of binary pulses. In contrast, Deisch discloses signal shaping circuits. These are totally different arts. Thus, it is submitted that Applicant's Claims 1 through 16 reciting a method for determining and apparatus for measuring characteristics of a bit stream of binary

pulses are clearly allowable in view of Deisch whether with reference to §102(b) or §103.

With reference to the Examiner's comment in 2A, Applicant states that Claims 1 through 8 recite an apparatus and Claims 9 through 16, method steps for defining a window comparator. As noted above, Deisch utterly fails to disclose control means defining a window comparator. Applicant recites such control apparatus and hence §102 is a wholly inappropriate rejection of the claims for defining a window comparator.

Figs. 7 and 9 (Deisch) do not show Applicant's recited control means defining a window comparator. The Deisch pulse shaping system (Fig. 12) discloses baseboard and output filters, 320, 305 that do not function as Applicant's recited control apparatus defining a window comparator. Specific reference is made to Deisch at col. 2, l. 40 through Col. 3, l. 7 and col. 4, ll. 49 through col. 5, l. 46, which do not disclose control apparatus for defining a window comparator. And, if Deisch were going to disclose such, it is respectfully submitted that it would appear at these sections in the disclosure. Therefore, Applicant's reasonably concludes that the recited control means and the recited method for defining a window comparator are clearly allowable in view of Deisch whether with reference to §102(b) or §103.

In response to the Examiner's comment 2B, Applicant cannot identify the Examiner's cited phrase "discussion of any characteristic of a bit steam" in his Response A to the Examiner's first Office Action. However, Applicant's Claims 1

through 16 each have a preamble reciting apparatus or method for measuring or determining characteristics of a bit stream of binary pulses. In addition, the claims recite apparatus and method of drawing eye diagrams defining bit stream characteristics. Deisch's pulse shaping circuits (Figs. 4 and 8) merely generate a straight line voltage or harmonics of the input voltages. The Deisch plotted graph (Fig. 5) merely illustrates a charge of capacitor C of the circuit Fig. 4. Deisch discloses pulse shaping concepts where filters (Fig. 12) would appear to delete characteristics of a bit stream of pulses appearing on a transmission facility. These same characteristics, deleted by the apparatus disclosed by Deisch, are measured and defined by the apparatus and method recited by Claims 1 through 16. Cleary, if for no other reason, Deisch can be fairly said to be a teaching in an opposite direction from the claimed invention here. As such §102 is wholly inappropriate as a grounds of rejection and the claims are clearly allowable whether in view of §102 or §103.

In response to the Examiner's comment 2C, Applicant cannot identify the Examiner's cited phrase "discussion of any characteristic of a bit steam with an eye diagram". However, Applicant's Claims 1 through 16 each recite structure or method for drawing eye diagrams defining bit stream characteristics. Again, the Deisch circuits (Figs. 4 and 8) do not draw eye diagrams defining bit stream characteristics. Deisch (Fig. 5) discloses the charge appearing on the capacitor C, not eye diagrams (Fig. 4 circuit). Specifically Deisch at col. 2, l. 40 through Co. 3, l. 67 does not disclose

generating eye diagrams defining bit stream characteristics. Again Claims 1 through 16 clearly recite structure or method for drawing eye diagrams defining bit stream characteristics. Applicant reasonably concludes §102 is wholly inappropriate as a grounds of rejection and the claims are clearly allowable whether in view of §102 or §103.

With regard to Examiner's comment 2D, Applicant's state that Claims 1 through 8 recite logic structure for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom. Again, Deisch (Fig. 7) is a plotted graph showing capacitor C voltages in response to operation of switches S1 and S2 of his Fig. 6 circuit wherein the capacitor charge and discharge voltages are added to create a straight line output voltage S_{OUT} and does not show Applicant's drawn eye diagrams. Deisch (Fig 8) is merely a signal pulse shaping circuit that apparently shapes a digital pulse such as shown in Fig. 9A into a basic harmonic waveform such as is shown in Fig. 9G. The Deisch's circuit (Fig.12) discloses at most the shaping of binary pulses wherein higher frequency components defining specific characteristics of the binary pulses are filtered out such that only shaped pulses of the basic harmonic frequency are present. Note his filters in the receiver circuit that appear to delete the higher frequencies defining the characteristics of the input binary pulses. Nowhere is there disclosed in Deisch, Applicant's recited logic structure for accumulating event counts of

the bit stream pulses falling within points inside a window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom.

With respect to Examiner's comment 2E, Applicant's states that Claims 2 through 6, 7, 8. 11 through 14, 15 and 16 recite structure and method for creating a voltage threshold window that moves between a maximum and minimum voltage. None of the circuits illustrated or described in Deisch (Figs. 4, 6, 8, 10 and 12) disclose any of features recited in these claims. And, that is not surprising since Deisch is a disclosure in an entirely different direction. The plotted graphs (Deisch, Fig. 7) at most disclose outputs of the circuit of Fig. 6 (Deisch), the baseboard filter 320 (Fig. 12). There is simply no disclosure relating to Applicant's recited structure and method for creating a voltage threshold window that moves between a maximum and minimum voltage.

With respect to Examiner's comment 2F, Applicant's states that Claims 4 through 6 and 8 recite counter structure for accumulating counts of the detected binary pulse voltage levels. The Examiner states Deisch discloses "counter means to detect accumulating counts of binary pulses" in Fig. 7, 8, unit 106, 108, 104, 122, Fig. 9 through 11. As noted above, Figs 7, 9 and 11 (Deisch) are plotted graphs of the capacitor voltages in the circuits illustrated in Figs. 6, 8 and 10. These plotted graphs of Deisch do not and could not disclose counter structures. Deisch at col. 5, ll. 1 and 2 states that the circuit of Fig. 8, unit 106, is a one bit shift register, not a counter

structure, which shifts pulses on lead 104 (not count) therethrough, in response to clock pulses on lead 108. Similarly and as noted in detail above, Deisch does not disclose a second counter structure as recited in Applicant's Claims 5 and 8.

In response to the Examiner's comment 2G; Applicant cannot identify the Examiner's cited phrase "display windows comparator with eye diagram" in his Response A to the Examiner's first Office Action. Applicant's Claims 1 through 16 recite structure and method defining a window comparator, accumulating event counts of the bit stream pulses falling within points inside the window comparator and drawing eye diagrams therefrom defining characteristics of a bit stream of binary pulses. The Examiner states that "Deisch discloses 'display windows comparator with eye diagram' in Fig. 5, Fig. 8, unit 122, Fig. 10, unit 169.". Deisch's plotted graph, Fig. 5, contrary to the Examiner's statement, does not disclose Applicant's recited window nor does it show eye diagrams. Deisch's plotted graph of his Fig. 5 illustrates the voltage of capacitor C in his circuit of Fig. 4. It is submitted that the output lead of this idealized circuit would not be an eye diagram but as stated in Deisch at col. 4, ll. 10 through 14, a constant voltage shown as straight line S_{OUT}.

Deisch's pulse shaping circuits set forth in his Figs 8 and 10 have output leads, not units, 122 and 169 that generate, not eye diagrams, but fundamental harmonic wave output voltages set forth in Figs. 9G and 11B, respectively. Thus, Deisch's reference does not disclose, teach, anticipate or even suggest Applicant's recited

structure and method set forth in Claims 1 through 16 for defining a window comparator, accumulating event counts of the bit stream pulses falling within points inside the window comparator and drawing eye diagrams therefrom defining characteristics of a bit stream of binary pulses.

In response to the Examiner's comment 2H, it is submitted that Applicant's above comments and those previously set forth in Response A comments clearly and convincingly demonstrate that Applicant's Claims 1 through 16 are neither disclosed, taught, anticipated nor even suggested by the Deisch reference and are therefore clearly allowable under 35 U.S.C. §1 et seq.

CONCLUSION

Applicant having answered each and every ground of rejection and/or objection as set forth by the Examiner respectfully submits that the above case is now clearly in condition for allowance based upon the remarks as set forth above. Applicants now request that this Response B be considered and that it be entered on the record. Applicant requests that if the Examiner has further questions or wishes to clear up any matter that he is invited to telephone the undersigned at the number given below.
If any questions should arise with respect to the above remarks, or if it would in any way

expedite the prosecution of this case, Applicants' attorney would appreciate a telephone call by telephoning (408)-965-4001.

Respectfully submitted

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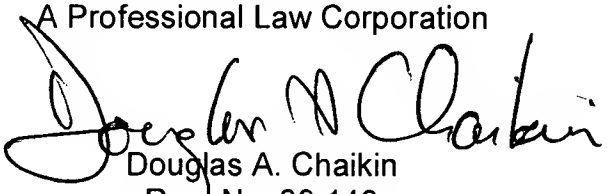

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